REMARKS

By this response claim 1 has been amended and claims 24-38 have been added. Claims 1-17 and 21-38 are pending. Claims 10-17 and 21-23 have been allowed. Reconsideration of the application is respectfully requested.

Newly added claims

The subject matter of claim 5, which has been objected to by the Examiner and indicated as including allowable subject matter, has been written into claim 1 from which it depends and submitted as new claim 24. Thus claim 24, and claims 25-29 which depend therefrom, are allowable for at least this reason.

Claims 30-38 have been added in response to the Examiner's comments at page 6, last paragraph of the pending office action. For example, claim 30 positively recites "removing the second conductive layer from over an entire width of the first conductive layer" and further recites "forming a silicide layer simultaneously on the entire width of the first conductive layer and over the second conductive layer." As the Examiner deemed the arguments with respect to original claim 1 unpersuasive for the reasons stated in the office action, and claim 30, insofar as it comprises the amended subject matter of original claim 1, overcomes the Examiner's reasons regarding the lack of persuasiveness of the arguments, it is submitted the arguments should now be persuasive with regard to claim 30. Claim 30 and claims 31-38 which depend therefrom, are therefore in condition for allowance.

Rejections under 35 USC §102(e)

Claims 1-4 and 8 have been rejected under 35 USC §102(e) over Chiang et al., US Pat. 6,383,863. Chiang recites the formation of a semiconductor device in which a silicide layer 20 is simultaneously formed over a polysilicon transistor gate 4 and a capacitor top plate 18 as depicted in FIG. 9.

The Examiner uses the formation of polysilicon layer 4 (FIG. 2 of Chiang) and the formation of the silicon dioxide layer 5 to teach the formation of the "first conductive layer and at least one dielectric layer" respectively of present claim 1. The formation of dielectric layer 10 (FIG. 8) is used to teach the formation of the first dielectric spacer on the first sidewall and to teach the recited elements of present claim 1.

Claim 1 has been amended to more particularly indicate the formation of the first and second dielectric spacers on the sidewalls, wherein the sidewalls comprise "the at least one dielectric layer and the first conductive layer." Claim 1 as amended recites "...forming a first dielectric spacer on the at least one dielectric layer and on the first conductive layer of the first sidewall and a second dielectric spacer on the at least one dielectric layer and on the first conductive layer second sidewall to cause an upper surface of each sidewall to extend above an upper surface of the first and second spacers...".

The invention as presently claimed comprises novel differences over the disclosure of Chiang which render claim 1 allowable under 35 USC §102(e). For example, in FIG. 8 of Chiang, there is no apparent instance of forming first and second dielectric spacers "to cause an upper surface of each sidewall [i.e. sidewalls comprising conductive layer 4 and dielectric layer 6 and/or 5] to extend above an upper surface of the first and second spacers" [i.e. layer 10, as applied by the Examiner]. In all cases of the sidewalls which comprise both conductive layer 4 and dielectric layers 6 and/or 5, layer 10 (which the Examiner uses as the spacer) is formed to lie above the upper surface of the sidewall. With regard to FIG. 8, only the two center gates comprise two sidewalls formed by layers 4, 5, and 6, with the adjacent gates lateral to the two center gates comprising one sidewall each formed by layers 4, 5, and 6. In all these cases, layer 10 is above the upper surface of each sidewall. Thus Chiang fails to disclose "an upper surface of each sidewall is [caused] to extend above an upper surface of the first and second spacers," and claim 1 is therefore allowable over Chiang under 35 USC §102(e). Rejected claims 2-4 are allowable at least because they depend from an allowable base claim.

Rejections under 35 USC §103(a)

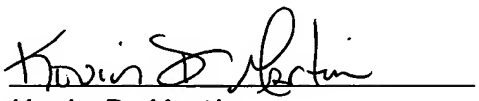
Claim 9 has been rejected under 35 USC §103(a) over Chiang and Shin (US 6,635,536).

As discussed relative to the rejection under 35 USC §102(e), Chiang and Shin in combination fail to teach or suggest forming first and second dielectric spacers "to cause an upper surface of each sidewall [i.e. sidewalls comprising conductive layer 4 and dielectric layer 6 and/or 5] to extend above an upper surface of the first and second spacers" [i.e. layer 10, as applied by the Examiner]. In all cases of the sidewalls which comprise both conductive layer 4 and dielectric layers 6 and/or 5, layer 10 (which the Examiner uses as the spacer) is formed to lie above the upper surface of the sidewall. Thus claim 9 is allowable over Chiang and Shin in combination under 35 USC §103(a).

Conclusion

If there are matters which may be clarified or resolved through a telephone call, the Examiner is cordially invited to contact the undersigned. This is believed to be a complete response to the Examiner's office action.

Respectfully submitted,



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